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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,391	12/01/2000	Edward Colles Nevill	550-189	1282

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EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,391	NEVILL, EDWARD COLLES	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the appeal brief filed on 4/18/05, PROSECUTION IS HEREBY REOPENED. The non-final action set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7 and 9-14 are rejected under 35 U.S.C. 102(e) as being anticipated by TREMBLEY (U.S. Patent 6,065,108).

As to claim 1, TREMBLAY teaches an apparatus for processing data, the apparatus comprising: a processor core (instruction and data processor); a main memory (associative memory / non-quick to quick translator cache) operable to store instruction words (instructions) and data words (data sets) (col. 24, lines 56-60); a data store (data set memory section / cache) operable to store words (data sets) from the main memory accessed by a data store port (via a bus connection 17) (see figure 6) of the processor core (col. 25, lines 23-35; col. 16, lines 1-12); an instruction store (instruction memory section / instruction cache) operable to store words (instruction identifiers) from the main memory accessed by an instruction store port (via a bus connection 15) (see figure 6; col. 7, lines 65-67) of the processor core; and an instruction interpreter operable to read instruction words from the instruction store (via determining whether the instruction corresponds the identifiers stored in the instruction memory section; via retrieving instructions to be decoded and executed) (col. 25, lines 47-54; col. 25, line 66 – col. 26, line 12; col. 12, lines 10-19); wherein the instruction interpreter is operable to modify a slow form instruction (non-quick instruction / retrieved instruction) within the instruction store to a fast form instruction (quick variant having the corresponding data set) of one or more possible fast form instructions and to write the fast form instruction to the data store (via when it is determined that there is no match, to initiate a trap such that the retrieved data set is written into the data set section corresponding to the instruction identifier thereby making the instruction quick) (col. 27, line 5 – col. 28, line 6; col. 28, line 48 – col. 29, line 14), the slow form instruction (non-quick instruction) and the fast form instruction (quick variant) having a common

functionality when executed by the interpreter (via the instruction is similar but the data set needed to execute the non-quick instruction is loaded thereby making the instruction quick) (col. 28, lines 29-40); and the instruction interpreter is operable upon reading a slow form instruction (non-quick instruction identifier / via retrieving instructions to be decoded and executed) from the instruction store to check for a corresponding fast form instruction (quick variant / data set) within the data store (data set memory section) and, if the fast form instruction (quick variant / data set) is present within the data store, then to execute the fast form instruction (quick variant of the non-quick instruction wherein the retrieved data set allows for quick execution) instead of the slow form instruction (non-quick instruction with no data set for quick execution) (col. 26, lines 32-45; col. 28, lines 10-40).

As to claim 2, TREMBLEY teaches the instruction interpreter is a hardware based instruction translator (col. 6, lines 7-12).

As to claim 3, TREMBLEY teaches the instruction interpreter is a software-based interpreter (col. 6, lines 7-12).

As to claim 4, TREMBLEY teaches the instruction interpreter is a combination of a hardware based instruction translator and a software based interpreter (col. 6, lines 7-12).

As to claim 5, TREMBLEY teaches the data store is a data cache (col. 16, lines 1-12). Therefore, it would be inherent to the teachings of TREMBLEY that the port used to communicate with the cache is a data cache port.

As to claim 6, TREMBLEY teaches the instruction store is an instruction cache (col. 7, lines 61-67; col. 12, lines 10-18). Therefore, it would be inherent to the teachings of TREMBLEY that the port used to communicate with the cache is an instruction cache port.

As to claim 7, TREMBLEY teaches the slow form instruction (non-quick instruction) results in an unresolved storage access request to one or more stored words (col. 2, line 61 – col. 3, line 6) and the fast form instruction (quick variant) results in a resolved storage access request to the one or more stored words (col. 14, line 65 – col. 15, line 20; col. 27, lines 51-62).

As to claim 9, TREMBLEY teaches the slow form instruction invokes an additional data processing procedure before completion (locating and retrieving data) (col. 2, line 61 – col. 3, line 6).

As to claim 10, TREMBLEY teaches the slow form instruction and the fast form instructions are Java Virtual Machine Instructions (col. 5, lines 28-32).

As to claim 11, TREMBLEY teaches the slow form instruction is: anewarray (col. 26, lines 15-20).

As to claim 12, TREMBLEY teaches the slow form instruction is anewarray (col. 26, lines 15-20) and enhancing the slow form instructions into quick variants hence fast form instructions. Therefore, it is inherent within the teachings of TREMBLEY that the fast form instruction is also a quick version of anewarray.

As to claim 13, TREMBLEY teaches the instruction interpreter translates Java Virtual Machine instructions to native instructions of the processor core (col. 6, lines 52 – col. 7, line 20; col. 6, lines 3-12).

As to claim 14, reference is made to a method that corresponds to the apparatus of claim 1 and is therefore met by the rejection of claim 1 above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over TREMBLEY (U.S. Patent 6,065,108).

As to claim 8, TREMBLEY teaches the slow form instruction requires one to locate and retrieve the data required which requires excessive cycles (col. 2, line 61 – col. 3, line 6) while a quick variant retrieves the pre-loaded data via a reference (numeric reference) and executes with the data generally in one cycle (col. 28, lines 21-40). Official Notice is taken in that it is well known in the art that in order to load data in memory the requesting entity has a symbolic reference to the element that loads and accesses a symbol table. Therefore, it would be obvious to one skilled in the art at the time of the invention to combine the teachings of TREMBLEY with the well-known concept of using a symbolic reference to load a required element in order to load necessary components for execution.

Relevant Prior Art of Record Cited, but not Relied Upon

"Compilers, Principles, Techniques and Tools" by Aho teaches the use and loading of elements through a symbol table.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 1, 2005

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER